ACTIVE-SNUBBING OR PASSIVE-SNUBBING FOR FAST SWITCHES?

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ABSTRACT

As power-switches improve, the primary function of switching-aid circuits changes from modifying the shape or rate-of-traverse of V-I loci within device safe-operating-areas (SOA's), to clamping transient current and voltage, at turn-on and turn-off, below peak current and voltage ratings. Also, as device ruggedness and device parameters are improved, or made less variable between devices and with operating conditions, active-snubbing or active-clamping becomes feasible, whereby the magnitude of peak-current at turn-on and peak-voltage at turn-off are limited by gate or drive-circuit control, or inherently by the devices themselves. Examples have been reported, however, none of these adequately compares active and passive snubbing, or exposes salient disadvantages in active-snubbing. A more objective appraisal of active-snubbing is attempted here, which uses as its basis for comparison; turn-on and turn-off commutation energy-loss, on-state energy-loss, overload capacity, and turn-on and turn-off delay.

Irrespective of whether active or passive snubbers or clamps are used, switch turn-off voltage-waveforms are often characterised by fast voltage-overshoot above the dc-supply voltage, or above the threshold-level of voltage-clamps, when used. High-frequency ringing inevitably follows turn-off, or the beginning or end of voltage-clamping. The cause and solution are examined.

KEYWORDS:
snubbers and clamps for fast-switches,
active-snubbing versus passive-snubbing,
efficient snubbers and voltage-clamps,
suppressing interference in power-stages.

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INTRODUCTION

Refinements in transistor and MOSFET technology have led to more rugged devices with better characteristics (1,2,3). Improvement in the speed of MOSFETs intrinsic diode (MOSFET-diode), by new cell-design (1) and minority-carrier lifetime-killing (2), has led manufacturers, to assert that MOSFET-diodes are usable as freewheel-diodes with little or no dv/dt-control, and to better specify their performance. Increased MOSFET dv/dt-withstand capability and diode-speed are often demonstrated by making comparisons between turn-on waveforms of old and new devices, operated in circuit fig.1. Normally, series-snubber inductance is not used, although stray-inductance is present. A similar evaluation of a cellular-transistor technology, but with external fast-diodes, has been reported (8), also, to show that improved ruggedness allows snubber-less operation. The implied conclusion of reports based on switch operation in fig.1 (4-8), is often that minimal switching-loss is achieved, by minimising series-snubber and stray-inductance in circuits; and by switching the devices as fast as possible, without exceeding peak-current ratings with high reverse diode-current. With little drain-inductance (fig.2A), peak switch-current is limited by controlling gate or drive dv/dt or di/dt. The gate or drive-control of turn-on di/dt, used in device evaluation, is called here active-snubbing to distinguish it from passive-component snubbing, or passive-snubbing. More generally, active snubbing or clamping can be defined as deliberately increasing switching energy-loss to decrease the rate-of-rise of freewheel-diode reverse-current to limit peak-current at turn-on, or to decrease the rate-of-rise of drain-voltage to limit overshoot magnitude at turn-off. 'Active' is used because di/dt or dv/dt are controlled by the switch drive-input (fig.2). Absorbing energy from stray-inductance by avalanching power-switches is also described as active-snubbing, because increased energy is also put into the switch; and conceptually switch-avalanche can be considered as gate-controlled (fig.2C). Equivalent passive-snubber circuits to those of fig.2 are given in fig.3. By comparing active-snubbing with passive-snubbing; it is possible to show that MOSFET manufacturers and users (4-8) are not recommending or evaluating the most efficient, or easiest to design circuits, although they are using the ones which require the least power-components on the switch output. What is generally demonstrated is that active-snubbing, as a mode of operation, is becoming feasible. Given the growing (4-8) interest in active-snubbing, a comparison with passive-snubbing is required which examines:

1. Device and circuit switching energy-loss at turn-on and turn-off, under different operating conditions;
2. Response of snubbers and clamps to current-overload and supply-voltage variation;
3. Affect of snubbing-type on other aspects of switch or power-stage performance.

ENERGY-LOSS OF di/dt CONTROL

When switching clamped-inductive loads, turn-on di/dt is reduced to limit peak freewheel-diode reverse-current below the Idm of the oncoming MOSFET. Fig.2A and 3A give active and passive forms of di/dt control. To analyse turn-on energy-loss, a complete switching-cycle is examined because the loss associated with turn-on of fig.3A is dissipated at turn-on and turn-off, unlike fig.2A. Fig.4 gives idealised waveforms for fig.2A and 3A and corresponding instantaneous-power plots. Crossover-times are considered negligible relative to total current rise-time. Table-1 summarises difference in commutation properties.

TABLE 1

ACTIVE-SNUBBING	PASSIVE-SNUBBING
All commutation-energy dissipated as heat-loss.	Significant stored energy (IoIrmL) returned to load.
Absolute and relative dissipated energy (fig.4 and 5).	
$Wona = \frac{Edc}{di/dt}\frac{(Ip + Irm)^2}{2}$	$Wonp = \frac{Edc}{di/dt}\frac{(Io^2 + Irm^2)}{2}$
$\frac{Wona}{Wonp} = 1 + 2(\frac{Irmn}{1 + Irmn^2})$, $\frac{Wona}{Wonp}(max)=2$, when $Irmn(=\frac{Irm}{Io})=1$	
All energy dissipated in the MOSFET.	Dissipated energy put into inductor-reset volt-clamp.
High instantaneous power-loss in MOSFET,	Instantaneous power-loss lower and more distributed
Snubbing via gate-drive. Gate-drive more complex.	Snubbing on power side. Reset clamp required.
High thermal-dissipation in MOSFET. MOSFET's thermal properties impose minimum on and off times	MOSFET's overvoltage capability and snubber inductor-reset impose minimum on and off times.
Thermal-circuit temperature-decay not easily predicted or observed.	Generally, current and voltage-decay predictable and observable.

Energy-loss associated with turn-on, is greater for active-snubbing than passive-snubbing, and is worst when Irm=Io. The reason is the return to the load of some energy initially stored in the inductor of the passive-snubber. Fig.4B shows when it occurs.

ENERGY-LOSS OF VOLTAGE CLAMPING

Distributed circuit-inductance exists in practical choppers as shown in fig.7A. Its effect is represented by fig.7B. At turn-off, a voltage-clamp is required to limit voltage-overshoot below MOSFET BVdss: the inductance would otherwise ring output-capacitance, Co, to a high voltage. Because stray-inductance is distributed, the voltage-clamp, of the type used in fig.3A to reset the series-snubber, is unsuitable. Stray-inductance forces the use of voltage-clamp types represented, in principle, in fig.8B and 8C. Clamping is applied directly across the switch and/or diode. Practical implementations are given in fig.6. From energy-loss considerations, fig.6D and 8C are similar. Recognising similarities in operation of fig.6 and 8 circuits gives quick insight into energy transfer at turn-on and turn-off (12).

In the same way as controlling di/dt limited peak-current at switch turn-on, limiting dv/dt, with a shunt-capacitor in fig.6A and 6B, constrains voltage-overshoot at turn-off. Circuits of the type in fig.6C, clamp voltage-overshoot directly. Table-2 gives the energy-loss in resetting stray-inductance at turn-off, with the RC-snubber, RCD-snubber, zener-diode principle, and soft voltage-clamp.

Table-2 shows that the soft voltage-clamp (fig.6D) is the most efficient voltage-clamp. Energy-loss at turn-off is all put into the resistor. Also, the soft

TABLE-2

RC-Snubber	RCD-Snubber	Zener-Diode	Soft-Volt-Clamp
Absolute energy-loss in a switching-cycle.			
$(2+\frac{1}{X^2})\frac{LIo^2}{2}$	$[1+(\frac{Edc^2}{Vos})]\frac{LIo^2}{2}$	$(1+\frac{Edc}{Vos})LIo^2$	$\frac{LIo^2}{2}$
$X = \frac{Io}{Edc}\sqrt{\frac{L}{C}}$ & Vos=rise on switch above Edc at turn-off.			
$2 + \frac{1}{X^2}$	$1 + (\frac{Edc}{Vos})^2$	$(1 + \frac{Edc}{Vos})$	1

Relative values of dissipated energy for various Vos

Vos(%)					X	Edc/Vos
10	10.7	101	11	1	0.34	10
20	5.6	26	6	1	0.53	5
30	4.1	12.1	4.3	1	0.70	3.3
40	3.4	7.3	3.5	1	0.84	2.5
50	3.0	5	3.0	1	1.00	2.0

X values from (9).

Io(%)				
100	1.0	1.0	1	1
75	1.8	1.8	1	1
50	4.0	4.0	1	1
25	16.0	16.0	1	1
10	100	100	1	1

Relative energy-loss as switch-current is reduced

voltage-clamp is the only clamp with dissipation, which is independent of the dc-rail voltage. The rest would have to be sized for energy-loss at the worst-case voltage. Optimisation of soft voltage-clamp components is given in (10). Note that, in principle, the RC-snubber dissipates marginally less energy than the zener-diode circuits. In practice, switch on-state current is usually often below the design value; and relative energy-loss becomes much greater when switch-current is reduced, as shown in Table-2. Also, RC-snubber performance is considerably affected by resistor parasitic-inductance, as will be shown later.

ENERGY-LOSS OF TURN-OFF OVERSHOOT CONTROL

Voltage-rise in fig.2B is reduced by negative feedback

TABLE-3

ACTIVE-SNUBBERS		PASSIVE-SNUBBERS	
Gate-Drain Capacitance	Avalanche Device	RC-Snubber	Soft volt -Clamp.
Absolute and relative values of turn-off energy-loss			
$(\frac{Edc^2}{Vos^2} + \frac{2Edc}{Vos} +1)\frac{LIo^2}{2}$	$(1+ \frac{Edc}{Vos})\frac{LIo^2}{2}$	$(2+ \frac{1}{X^2})\frac{LIo^2}{2}$	$\frac{LIo}{2}$
Vos = rise on switch above Edc at turn off & $X = \frac{Io}{E}\sqrt{\frac{L}{C}}$			
$(\frac{Edc^2}{Vos^2} + \frac{2Edc}{Vos} + 1)$	$(1 + \frac{Edc}{Vos})$	$(2 + \frac{1}{X^2})$	1

Relative energy-loss values for various Vos values.

Vos(%)			X		
10	121	11	(0.34)	10.7	1
20	31	6	(0.53)	5.6	1
30	15.4	4.3	(0.70)	4.1	1
40	9.8	3.5	(0.84)	3.4	1
50	7.0	3.0	(1.00)	3.0	1

In principle, all switching energy put into MOSFET.	In principle, switching energy put into snubber R.
High instantaneous power-loss in MOSFET.	Lower instantaneous power in resistor, not MOSFET.
Fast clamping of of high dv/dt.	Resistor and snubber-loop inductance gives overshoot
Greater production-spread, and nonlinear variation in parameters involved in the gate-drive circuit-design.	Variation in parameters better specified and more better specified, and more controllable & observable.
The last 3 rows of Table-1 apply here, also.	

through the gate-drain capacitor. Given high MOSFET transconductance, dVo/dt=Io/(1+R gfs)C; and a MOSFET output-capacitance of (1+R gfs)C, is simulated. Fig.6B gives the passive counterpart. Turn-off energy-loss for fig.2B, all of which is put into the MOSFET, is worse than the RCD-snubber. Table-3 summarises the features of 2 forms of active and passive-snubbing; and shows that, from energy-loss and ease-of-design considerations, MOSFET voltage-clamping, in principle, is best effected with soft voltage-clamps. Reducing MOSFET dVds/dt should be avoided: the energy-loss is so much greater than other methods. RC-snubbers prove less effective than avalanche-diodes, in practice, in hard-clamping very fast voltage over-shoot unless carefully designed, because of greater series parasitic-inductance. Inability to clamp very fast voltage wavefronts, when using MOSFET's with little repetitive avalanche capability, is one instance when active-snubbing must be used, prior to an external voltage-clamp taking effect.

Although the primary function of voltage snubbers or clamps is to limit overshoot which would otherwise cause device degradation or catastrophic failure, a secondary function is usually required; ie. damping high-frequency oscillation, which starts at the onset and/or termination of clamping. Generally, the better the clamp, eg. avalanche-diode with very low dynamic-resistance and parasitic-inductance, the more underdamped and higher the frequency of oscillations. Also, snubber-diode effective parallel-capacitance may neither adequately rectify nor impede ±10 MHz voltage ringing. While ringing does not cause immediate catastrophic device-failure, it does generally interfere with control-circuit operation and obscure the observation of device switching-performance. Overall system reliability inevitably suffers. That there is a problem, is often brought home by emi-emission measurements. Figure-9 gives snubbers likely to produce hf ringing. External zener-diode clamp, fig.9A, has dynamic-resistance and parasitic-inductance added in the equivalent-circuit. Once MOSFET Co is charged above Edc, Co-Lc resonance is excited to an extent dependent upon the applied dv/dt. When Ls discharge is complete, switch voltage falls below Vz and Co resonates with Ls. Rd is small, for hard voltage-clamping, and resonance in either mode is underdamped. Simple parallel-damping, by connecting a resistor across the MOSFET, gives high steady-state power-dissipation. The only practical solution is an RC-snubber across the MOSFET (fig.10). Figure-10, with Lc in place of Ls and only the RC-snubber across the MOSFET, is sufficiently accurate, if Lc>>Ls and Cn>>Co. McMurrays (11) RC-snubber oetimisation method can then be used. If the Co/Cn ratio and RC-snubber parasitic-inductance are not small, overshoot is significantly worse than predicted by (11). The soft voltage-clamp, fig.9C and 10C, reduces to a similar resonant-circuit as the zener-diode clamp.

The RC-snubber of fig.10D is designed to reset Ls in a well damped manner. R and C component values are optimised using fig.13 and the expressions in the Appendix. In practice, parasitic-components Lc and Co (fig.9D) worsen damping and voltage-overshoot. Fig.14-16 give curves of peak voltage-overshoot for some relative values of Co (assumed linear, Ctn=Con=Co/Cn) and Lc (Lcn=Lc/Ls). If Lc is initially assumed negligible, the affect of Co on overshoot can be seen. Fig.14 shows the increase for Con=0.2 and 0.5. As switch output-capacitance is increased from zero, peak-overshoot rises to a maximum and then decreases as Con is further increased (9). Damping continues to deteriorate progressively with rising Con. Since Co is set by the switch, raising RC-snubber capacitance to reduce the relative value of Co (ie. Ctn in fig.14 and Con in fig.15 & 16) is the easiest solution. Fig.16 gives peak-overshoot curves for 4 values of Lcn, (Lc/Ls) with fixed Con. Peak-overshoot for zero Lcn and Con is also given for comparison. Each Lcn value has a critical initial-current value, X, above which overshoot rises rapidly. Fig.15 shows that as Con decreases for constant Lcn the critical X value decreases. By implication, RC-snubber inductance is most effective in increasing overshoot in high-current low-voltage switches since X = (I/Edc)$\sqrt{}$Lc/Co, particularly, if device current-density is high and, therefore, output-capacitance is low. Regarding RC-snubber parasitic-inductance optimisation, it would seem possible to specify an upper limit, given a minimum for Co and values of operating current and voltage. Reducing inductance below the limit, other than to allow for tolerance in circuit parameters, would give little further improvement (fig.16).

ENERGY-LOSS WITH ON AND OFF AND MULTIPLE SNUBBERS

The previous analysis of snubbers does not give entirely accurate expressions for energy-loss; eg. stray-inductance, included in turn-off snubber analysis, was not included in turn-on snubber analysis, and yet it reduces turn-on energy-loss in MOSFETs. Also, the discharge-current of turn-off-snubber capacitors, which adds to turn-on current transients, was ignored in turn-on analysis. The energy-loss expressions presented are just adequate to firstly indicate whether active or passive snubbing is more efficient, and secondly by roughly how much. The conclusions are generally unaltered when both turn-on and turn-off snubbers are added to switches.

TURN-OFF SNUBBER EFFECTIVENESS WITH CURRENT OVERLOAD

If turn-off snubbers are designed to give protection only for maximum load-current, MOSFET or switch failure may occur if turn-off is attempted during the turn-on current transient (fig.4) when peak-current up to 4 times the average-current value is, in principle, possible. As shown below, even allowing a 100% safety margin is inadequate when turn-off clamp-design is based on maximum average-load-current.

TABLE 4

Load-Current	Peak Switch-Current	Wp/WL
No margin, Io	4 Io	16
50% margin, 1.5 Io	1.5 Io	7
100% margin, 2 Io	4 Io	4
Energy stored in Ltotal at diode-recovery peak,	$Wp = \frac{1}{2}$ L total $(4\ Io)^2$	

Energy stored in Ltotal due to Io, $Wo = \frac{1}{2}$ L total Io^2

Using the non-repetitive avalanche-energy capability of MOSFET's seems permissible (1) for devices which have specified values, providing repeated narrow on-pulses are detected as a fault condition. Minimum on-time must include the decay-time of Irm in snubber-inductance. Table-4 gives examples of inductance values, below which snubber plus stray inductance, Ltotal, must be set to uphold avalanche ratings for a few devices. The inductance used in practice is usually far less.

TABLE 5

		25°C	------100°C-------			
MOSFET	BVdss(V)	Id(A)	Id(A)	Idm(A)	Eas(mJ)	Lmax(μH)
IRF640	200	18	11	44	95	20
IRF740	400	10	6.3	25.2	75	47
IRF840	500	8	5.1	20.4	75	72

Avalanche energy, Eas = (BVdss/(BVdss-Edc))(L Io^2/2)

=>Lmax = 2xEas/((BVdss-Edc)/(BVdss Io^2))

If device used at < 80% of BVdss, Lmax = 0.4 Eas/Io^2

Apart from zener-diode voltage-clamps, the current-overload capability of other clamps in Table-2 is poor, ie. voltage-overshoot increases significantly with multiples of average switch-current (Table-5).

To increase the capability of the capacitor-based voltage-clamps to clamp Vos<10% for 4Io requires a 16-times increase in capacitor value, producing a 4-times increase in capacitor reset-time. There is therefore a

TABLE 6

	RC-snubber	RCD-Snubber	Zener-Diode	Soft-Volt-Clamp
	Vos(%EDC)	Vos	Vos	Vos
Io	10	10	dependent	10
2Io	30	20	on dynamic	20
3Io	80	30	resistance	30
4Io	70	40		40

Increase in Vos for k x Io above design value of Io.

considerable advantage in widening minimum on-times to include turn-on current transients; and using rugged, well proven, MOSFET's to safely absorb excess energy during infrequent fault-conditions.

OTHER BASIS FOR SNUBBER COMPARISON

Active turn-on di/dt or turn-off dv/dt control (figs.2A and 2B) is produced by reducing dVgs/dt. MOSFET's pass through the linear-operating-region more slowly in consequence. In active-snubbing circuits, dId/dt and dVds/dt, and other MOSFET parameters are related by complex expressions, which comprise voltage (Crss), current (gfs) and temperature (gfs, Vgs(th)) dependent parameters. Also, these, and other less variable parameters, generally have production tolerances exceeding 10%, making precise design and performance-prediction difficult. However, even if precise design were possible, active-snubbing has several other disadvantages, viz increased turn-on and turn-off delay, increased MOSFET on-state loss, and power-circuits are less immune to commutation-noise. Comparison of fig.11 and 12 illustrates these. Delays t0-t1, are not easily reduced in fig.11 without changing di/dt and dVds/dt. In fig.12 they are independently variable. Between t2-t3 and t0-t1 (fig11), Vds or Rds(on) continues to be modulated by Vgs during the latter part of the Vgs rise. In fig.12 the lowest Rds(on) value is attained early on in the turn-on transient, and t0-t1 can be short. Finally, the fast low-impedance gate-drive used with passive-snubbers is more immune to uncontrolled switching-noise. Switching-noise at t2 (fig.12) is fed back to the gate with greater attenuation with low-impedance drives. Other noise occurs when the MOSFET is hard-on or hard-off. The disadvantages of active-snubbing become more pronounced as dc-rail voltage and chopping-frequency are increased. Diode reverse-recovery charge increases significantly and delay values relative to switching-period are much worse.

CONCLUSIONS

1. Voltage and current clamping is required to some extent with any switch, even MOSFETs to overcome freewheel-diode stored-charge and stray-inductance; one of which dominates at high-current or high-voltage.
2. Snubbing is, in principle, more efficiently performed with passive-snubbers, acting directly on switch outputs rather than with active-snubbers acting indirectly on switch outputs via gate control. Commutation power-loss is much less and primarily put into resistors rather than the MOSFETs. Also, snubber design-equations contain less current, voltage and temperature variability and production-tolerance.
3. Capacitor-based turn-off snubbers or clamps have poor overload capability. Voltage-overshoot increases directly with current: Vos/Vos(rated) = k(Ioverload/Id), where k≥1. Active-snubbing, ie. switch avalanche, offers the most efficient and certain overload protection; providing the MOSFET has a specified guaranteed-minimum single-pulse-avalanche-energy rating which is not exceeded by repetitive overload events. Such MOSFETs are inherently well protected when turn-off occurs during turn-on current-transients due to freewheel-diodes or during a load-impedance fault. More efficient "load-current" clamps can then used for repetitive operation.
4. Factors such as switching delay, on-state power-loss and noise immunity should also be considered when comparing active and passive snubbers, rather than just commutation power-loss.

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APPENDIX

$$C = L\left(\frac{I}{Edc\ X}\right)^2 \qquad \text{initial-current factor, } X = \frac{I}{Edc}\sqrt{\frac{L}{C}}$$

$$R = \frac{2\ \zeta\ Edc\ X}{I} \qquad \text{damping-factor, } \zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$$

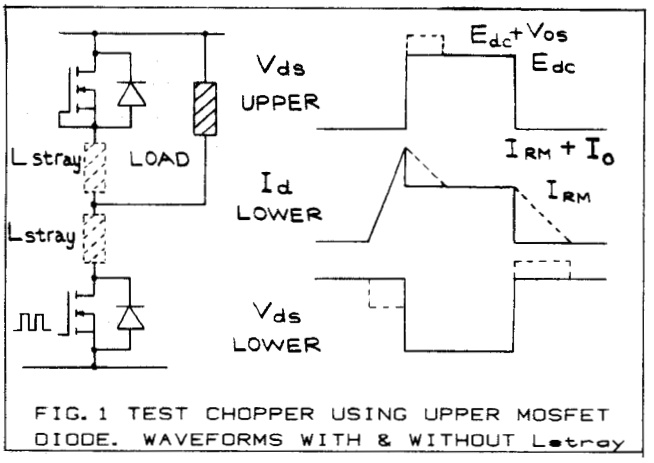


FIG. 1 TEST CHOPPER USING UPPER MOSFET DIODE. WAVEFORMS WITH & WITHOUT Lstray

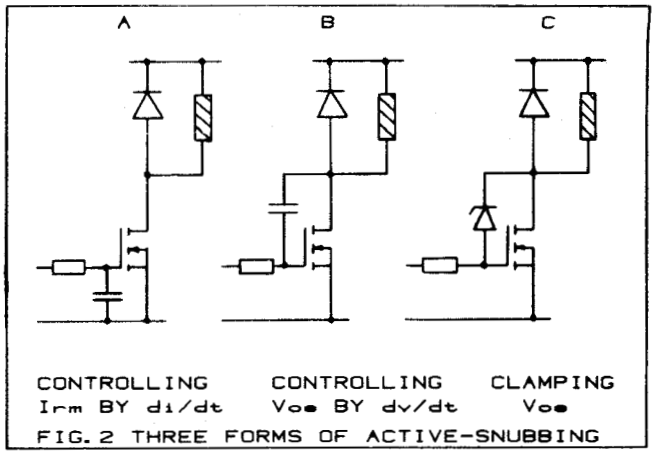


FIG. 2 THREE FORMS OF ACTIVE-SNUBBING

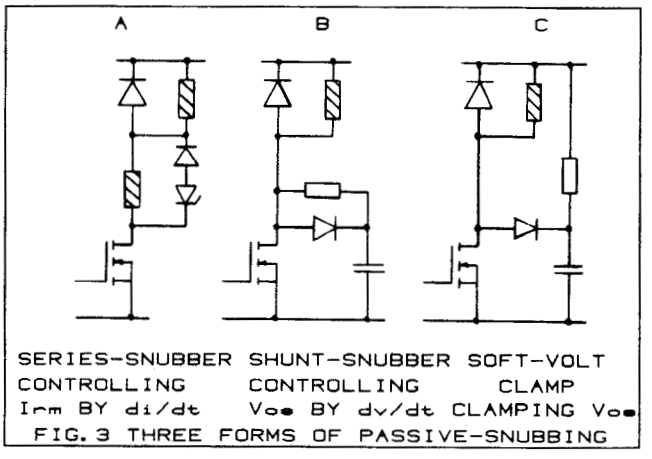
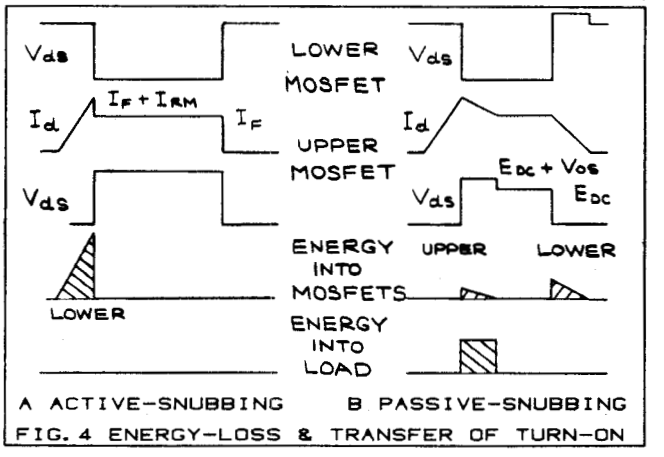


FIG. 3 THREE FORMS OF PASSIVE-SNUBBING



A ACTIVE-SNUBBING B PASSIVE-SNUBBING

FIG. 4 ENERGY-LOSS & TRANSFER OF TURN-ON

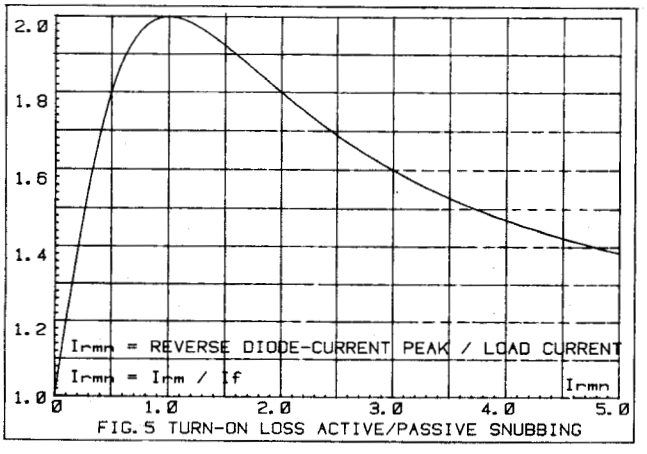


FIG. 5 TURN-ON LOSS ACTIVE/PASSIVE SNUBBING

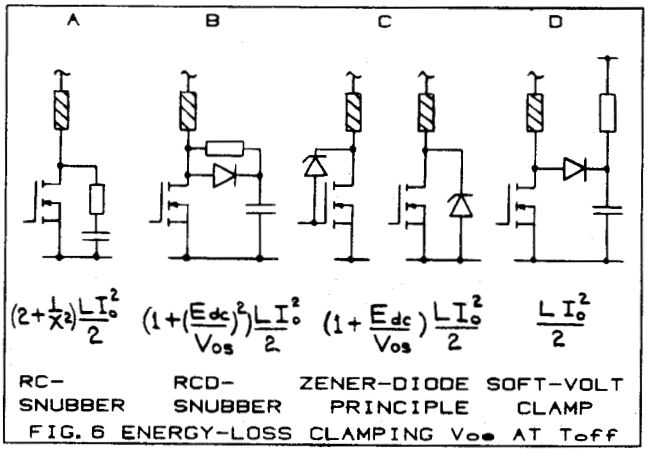


FIG. 6 ENERGY-LOSS CLAMPING Voe AT Toff

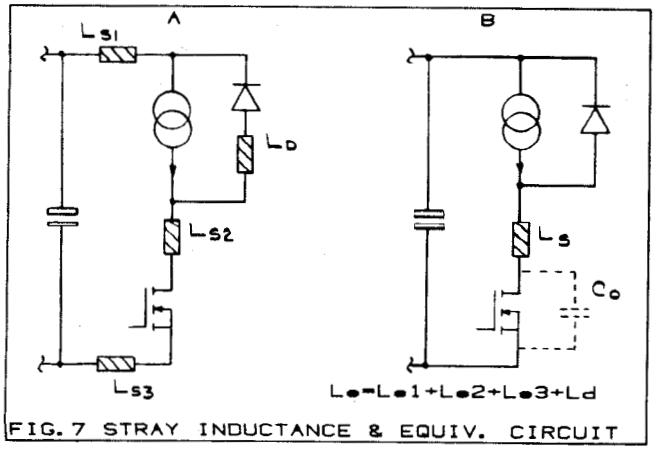


FIG. 7 STRAY INDUCTANCE & EQUIV. CIRCUIT

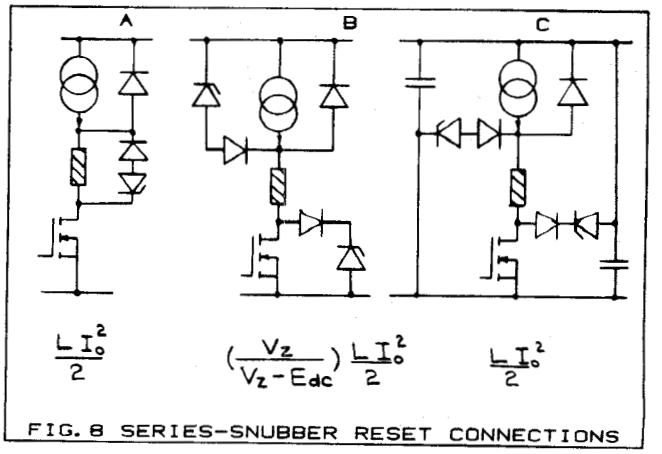


FIG. 8 SERIES-SNUBBER RESET CONNECTIONS

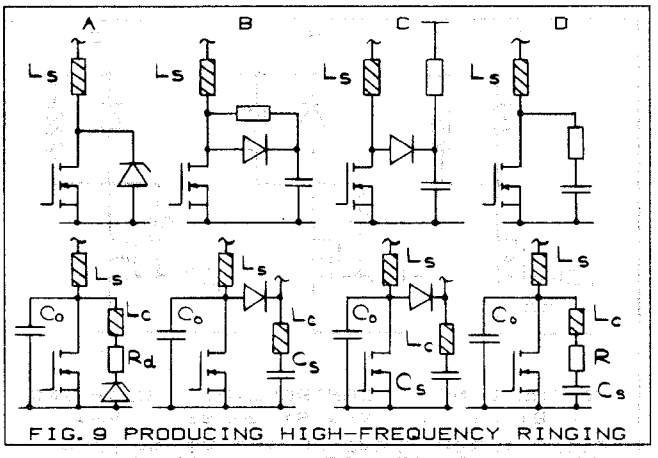


FIG. 9 PRODUCING HIGH-FREQUENCY RINGING

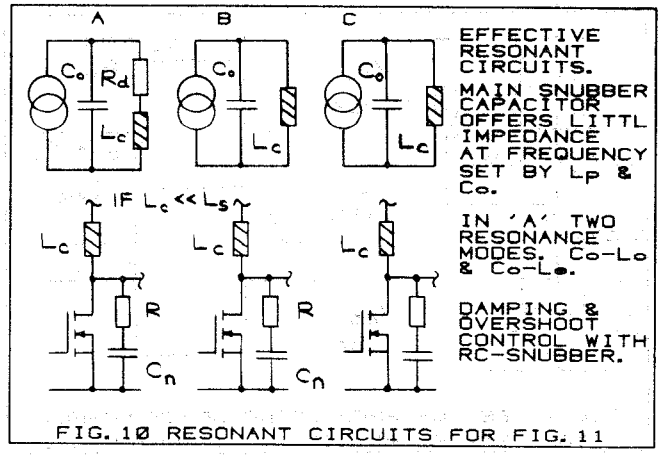


FIG. 10 RESONANT CIRCUITS FOR FIG. 11

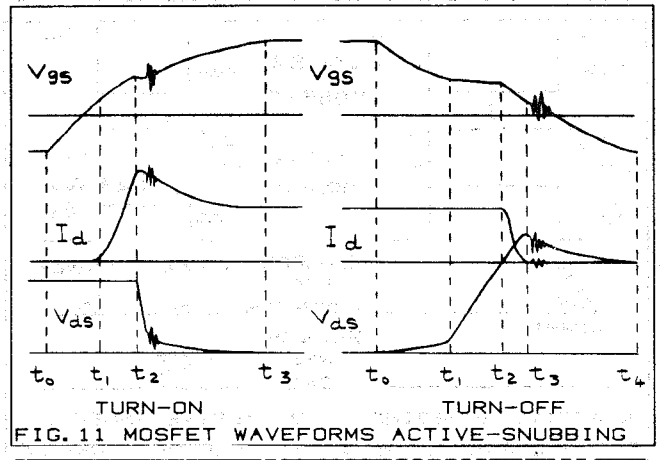


FIG. 11 MOSFET WAVEFORMS ACTIVE-SNUBBING

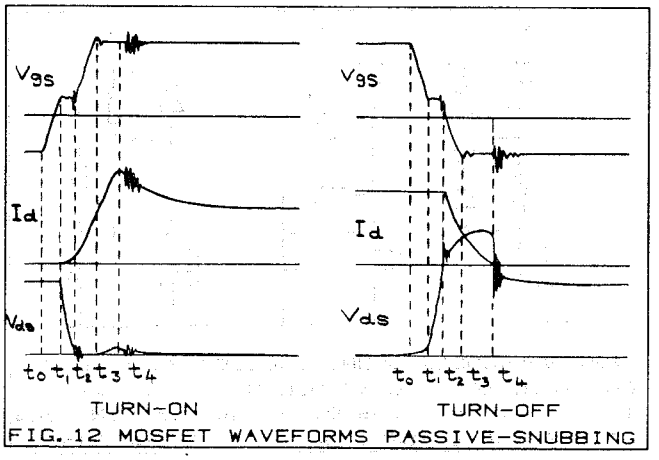


FIG. 12 MOSFET WAVEFORMS PASSIVE-SNUBBING

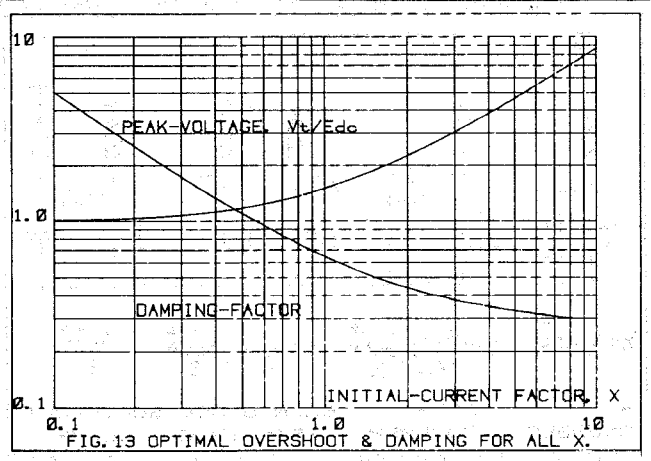


FIG. 13 OPTIMAL OVERSHOOT & DAMPING FOR ALL X.

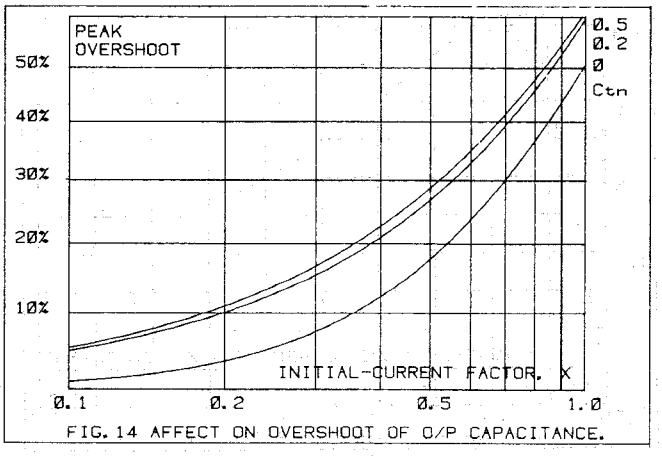


FIG. 14 AFFECT ON OVERSHOOT OF O/P CAPACITANCE.

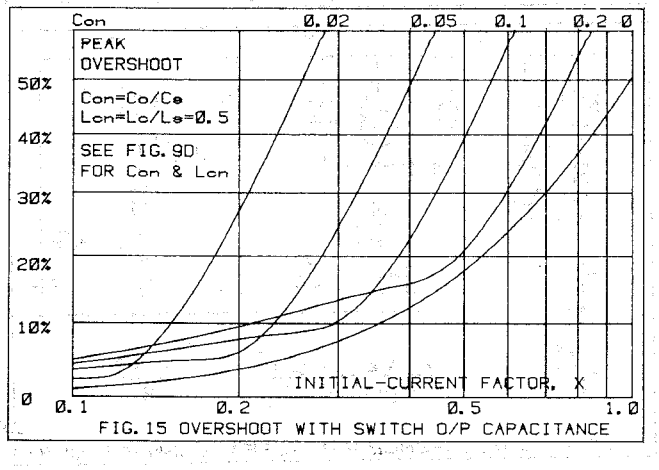


FIG. 15 OVERSHOOT WITH SWITCH O/P CAPACITANCE

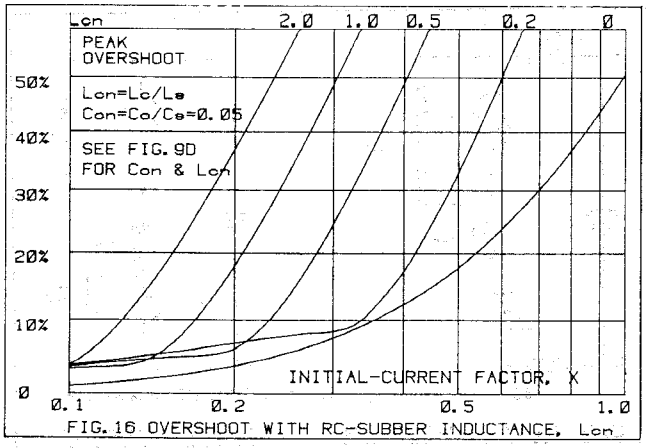


FIG. 16 OVERSHOOT WITH RC-SUBBER INDUCTANCE, Lon